port, and being operative to amplify said input signal by way of a third gain stage, said third gain stage having an output thereof coupled to said output port, so as to be combined with signals amplified by said first and second gain stages and provided at said output terminal of said output transistor.

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7. The amplifier architecture according to claim 6, wherein said third amplification path has a bandwidth that overlaps the bandwidth of said first amplification path.

8. The amplifier architecture according to claim 7, wherein said second amplification loop has a bandwidth on the order of decade lower than bandwidths of said first and third amplification loops.

9. An amplifier architecture comprising:

an input port to which a signal to be amplified is coupled;

an output port from which an amplified signal is derived;

a first amplification path coupled between said input port and said output port and including a first gain stage;

an output transistor coupled in voltage follower configuration having a control terminal coupled to said first gain stage and an output terminal coupled to said output port;